IN THE CLAIMS

Please replace all prior versions, and listings, of claims in the application with the following list of claims:

1. (Currently Amended) A linear regulator having an output stage comprising first and second P-channel MOS transistors serially connected between a first D.C. supply terminal and an output terminal providing a regulated output voltage, and a circuit for controlling the first and second transistors capable of providing said first and second transistors with first and second control signals as a function of the output voltage and [[to]] the voltage at the midpoint of the series connection.

2. (Original) The regulator of claim 1, wherein the control circuit comprises an input/output circuit and a reference circuit, the input/output circuit comprising:

a first input, receiving a first voltage reference provided by said reference circuit;

a second input, connected to said output terminal;

a third input receiving a second voltage reference provided by said reference circuit;

a fourth input connected to said midpoint;

a first output connected to the gate of the first transistor; and

a second output connected to the gate of the second transistor.

3. (Original) The method of claim 2, wherein the input/output circuit is a double differential comparator with four inputs and two outputs.

4. (Original) The regulator of claim 2, wherein the input/output circuit comprises first and second differential comparators with two inputs and two outputs, the input terminals of the first differential comparator being the first and second input terminals of the input/output circuit and its output being the second output of said input/output circuit; and the input terminals of the second differential comparator being the third and fourth input terminals of said

input/output circuit and its output being the first output thereof.

5. (Currently Amended) The regulator of claim 4, wherein the first differential comparator comprises an input/output stage and an output stage, said input output stage comprising two differential branches, each of which comprises a P-channel MOS transistor connected in series with a [[fist]] first N-channel MOS transistor, the sources of the P-channel transistors being interconnected to an output terminal of a current source having an input terminal connected to said D.C. supply terminal, the sources of the first N-channel transistors being interconnected to a ground terminal, the gates of the N-channel MOS transistors being interconnected, the gates of the P-channel transistors forming the first and second input terminals of the input/output circuit, the gate of said first N-channel MOS transistor of the branch comprising the first input being connected to its drain, the midpoint of connection of the drains of the complementary transistors of the other branch being connected to the gate of a second N-channel MOS transistor connected, in said output stage, in series between the supply terminals, with a first impedance, the midpoint of the series connection of said first impedance and of the second transistor forming the output terminal of said first differential comparator.

6. (Original) The regulator of claim 5, wherein the second differential comparator is comprised of two symmetrical differential branches, each formed of the series connection of a second impedance and of a third N-channel MOS transistor, respectively, the sources of the third N-channel transistors being interconnected to the drain of a fourth N-channel MOS transistor having its source connected to ground, the gate of the fourth N-channel transistor being connected to the gate of the second N-channel MOS transistor of the output stage of the first differential comparator.

7. (New) A linear regulator having an output stage comprising first and second P-channel MOS transistors serially connected between a first terminal and an output terminal to provide a regulated output voltage, and a circuit that controls the first and second transistors capable of providing said first and second transistors with first and second control signals as a

function of the output voltage and the voltage at the midpoint of the series connection.

8. (New) The regulator of claim 7, wherein the control circuit comprises an input/output circuit and a reference circuit, the input/output circuit comprising:

a first input, receiving a first voltage reference provided by said reference circuit;

a second input, connected to said output terminal;

a third input receiving a second voltage reference provided by said reference circuit;

a fourth input connected to said midpoint;

a first output connected to the gate of the first transistor; and

a second output connected to the gate of the second transistor.

9. (New) The method of claim 8, wherein the input/output circuit is a double differential comparator with four inputs and two outputs.

10. (New) The regulator of claim 8, wherein the input/output circuit comprises first and second differential comparators with two inputs and two outputs, the input terminals of the first differential comparator being the first and second input terminals of the input/output circuit and its output being the second output of said input/output circuit; and the input terminals of the second differential comparator being the third and fourth input terminals of said input/output circuit and its output being the first output thereof.

11. (New) The regulator of claim 10, wherein the first differential comparator comprises an input/output stage and an output stage, said input output stage comprising two differential branches, each of which comprises a P-channel MOS transistor connected in series with a first N-channel MOS transistor, the sources of the P-channel transistors being interconnected to an output terminal of a current source having an input terminal connected to said first terminal, the sources of the first N-channel transistors being interconnected to a ground terminal, the gates of the N-channel MOS transistors being interconnected, the gates of the P-channel transistors forming the first and second input terminals of the input/output circuit, the

gate of said first N-channel MOS transistor of the branch comprising the first input being connected to its drain, the midpoint of connection of the drains of the complementary transistors of the other branch being connected to the gate of a second N-channel MOS transistor connected, in said output stage, in series between the supply terminals, with a first impedance, the midpoint of the series connection of said first impedance and of the second transistor forming the output terminal of said first differential comparator.

12. (New) The regulator of claim 11, wherein the second differential comparator is comprised of two symmetrical differential branches, each formed of the series connection of a second impedance and of a third N-channel MOS transistor, respectively, the sources of the third N-channel transistors being interconnected to the drain of a fourth N-channel MOS transistor having its source connected to ground, the gate of the fourth N-channel transistor being connected to the gate of the second N-channel MOS transistor of the output stage of the first differential comparator.